

• General Description

It combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.

• Features

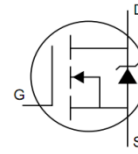
- Advance high cell density Trench technology
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance

• Application

- SMPS 2nd Synchronous Rectifier
- BLDC Motor driver

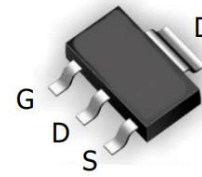
• Product Summary

$V_{DS} = 60V$



$R_{DS(ON)} = 50m\Omega$

$I_D = 9A$


SOT-223
• Ordering Information:

Part NO.	ZM500N06E
Marking	500N06
Packing Information	REEL TAPE
Basic ordering unit (pcs)	3000

• Absolute Maximum Ratings ($T_c = 25^\circ C$)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	$I_D @ T_C = 25^\circ C$	9.0	A
	$I_D @ T_C = 75^\circ C$	6.8	A
	$I_D @ T_C = 100^\circ C$	5.6	A
Pulsed Drain Current ^①	I_{DM}	27	A
Total Power Dissipation	$P_D @ T_C = 25^\circ C$	8	W
Total Power Dissipation ^②	$P_D @ T_A = 25^\circ C$	1	W
Operating Junction Temperature	T_J	-55 to 150	$^\circ C$
Storage Temperature	T_{STG}	-55 to 150	$^\circ C$
Single Pulse Avalanche Energy @ $L = 0.1mH$	E_{AS}	10	mJ
ESD Level (HBM)		CLASS 1B	

•Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case ^②	R _{thJC}	-	-	15	° C/W
Thermal resistance, junction - ambient	R _{thJA}	-	-	120	° C/W
Soldering temperature, wavesoldering for 10s	T _{sold}	-	-	265	° C

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = -250uA	60			V
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250uA	1.2		2.5	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} = 60V, V _{GS} = 0V			1.0	uA
Gate- Source Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V			±100	nA
Static Drain-source On Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 8A		50	65	mΩ
		V _{GS} = 4.5V, I _D = 6A		62	85	mΩ
Forward Transconductance	g _{FS}	V _{DS} = 10V, I _D = 5A		4		s
Source-drain voltage	V _{SD}	I _S = 8A			1.28	V

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Gate Resistance	R _g	f = 1MHz		1.9		Ω
Input capacitance	C _{iss}	f = 1MHz	-	823	-	pF
Output capacitance	C _{oss}		-	33	-	
Reverse transfer capacitance	C _{rss}		-	19	-	

•Gate Charge characteristics(T_a = 25°C)

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Total gate charge	Q _g	V _{DD} = 25V	-	11	-	nC
Gate - Source charge	Q _{gs}	I _D = 8A	-	2.5	-	
Gate - Drain charge	Q _{gd}	V _{GS} = 10V	-	1.5	-	

Fig.1 Gate-Charge Characteristics

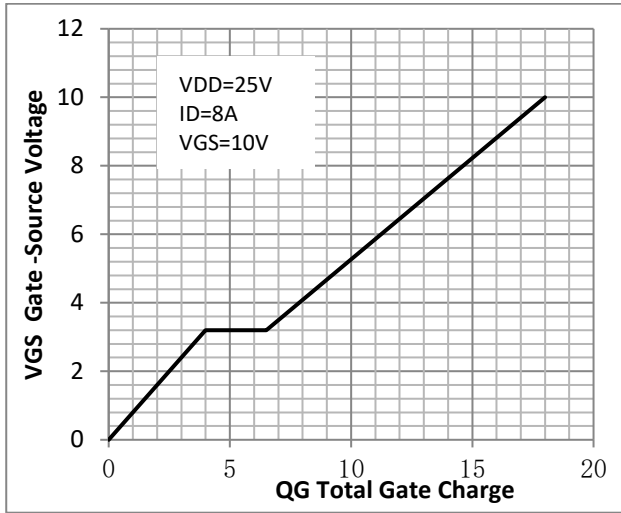


Fig.2 Capacitance Characteristics

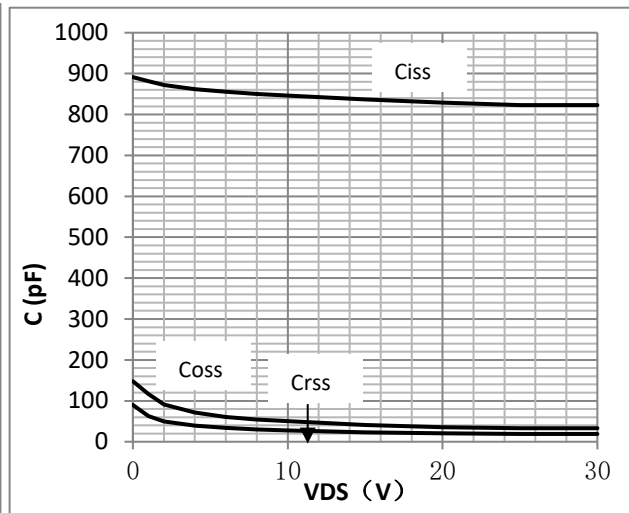


Fig.3 Power Dissipation Derating Curve

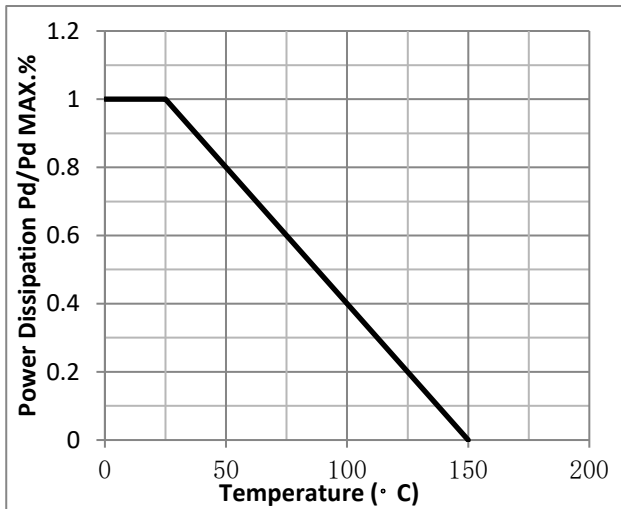


Fig.2 Typical output Characteristics

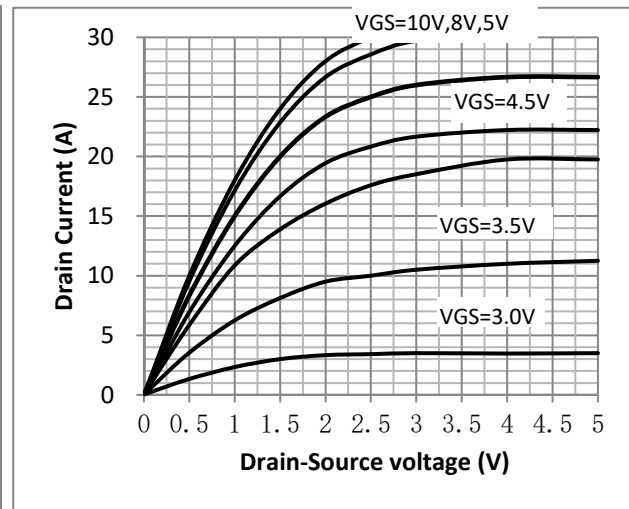


Fig.3 Threshold Voltage V.S Junction Temperature

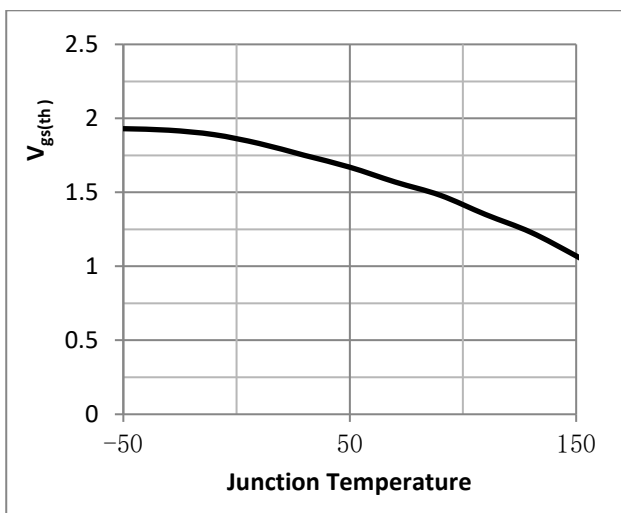


Fig.4 Resistance V.S Drain Current

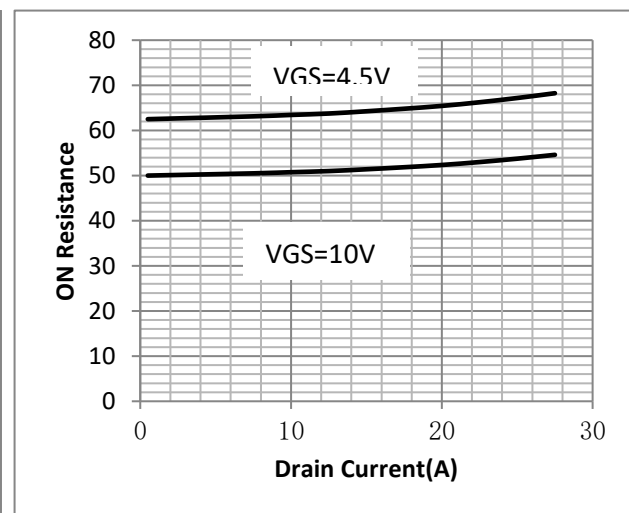


Fig.5 On-Resistance VS Gate Source Voltage

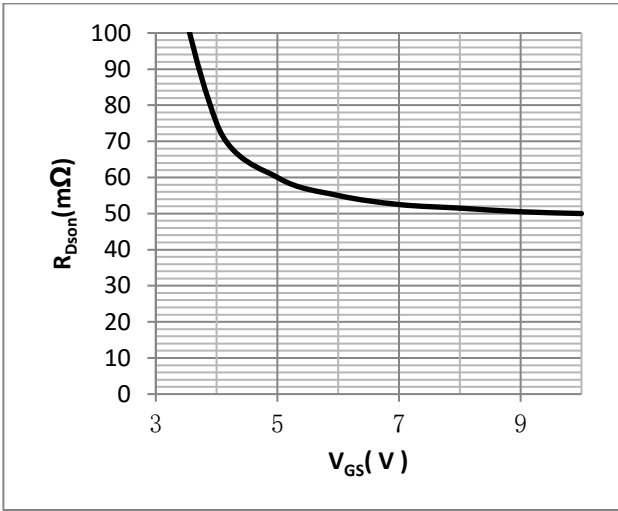


Fig.6 On-Resistance V.S Junction Temperature

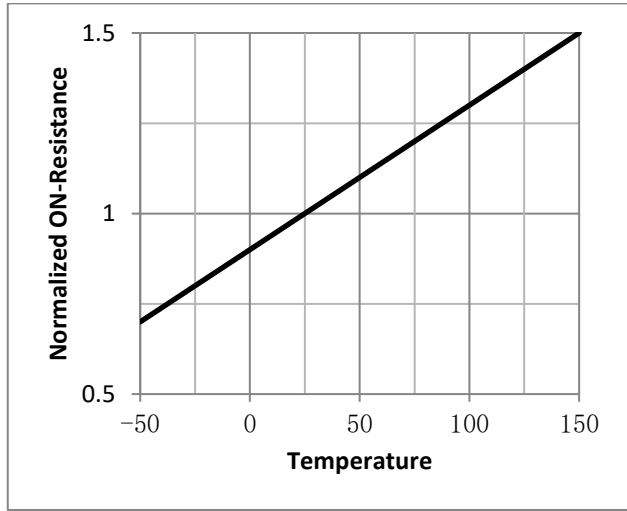


Fig.9 SOA Maximum Safe Operating Area

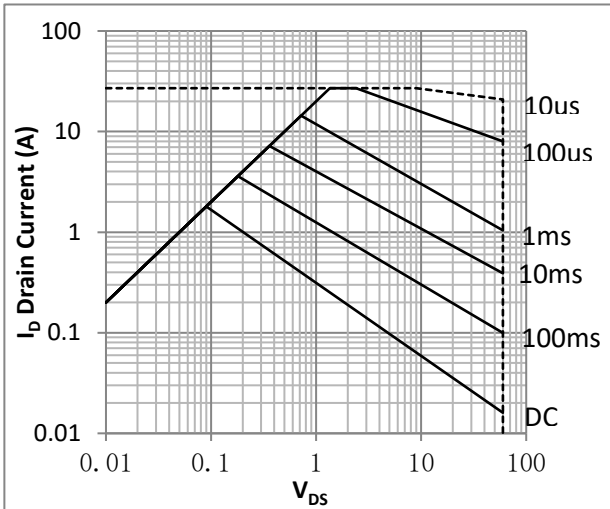


Fig.10 I_D-Junction Temperature

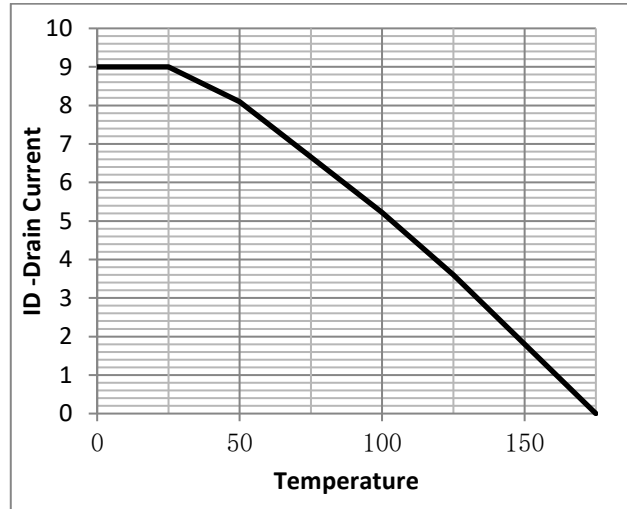


Figure 11. Diode Forward Voltage vs. Current

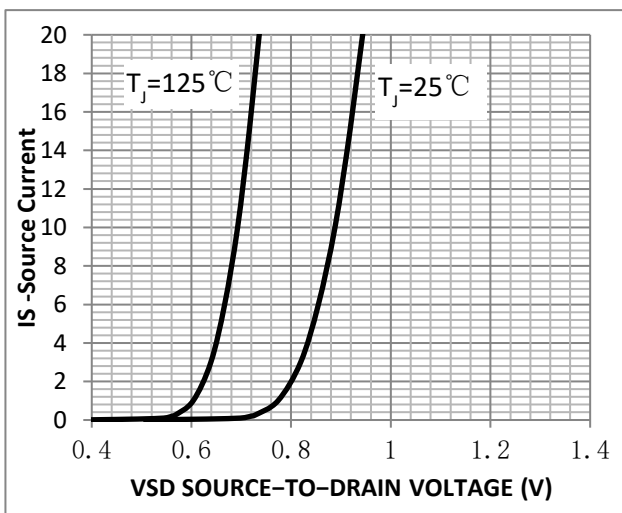


Figure 12. Transfer Characteristics

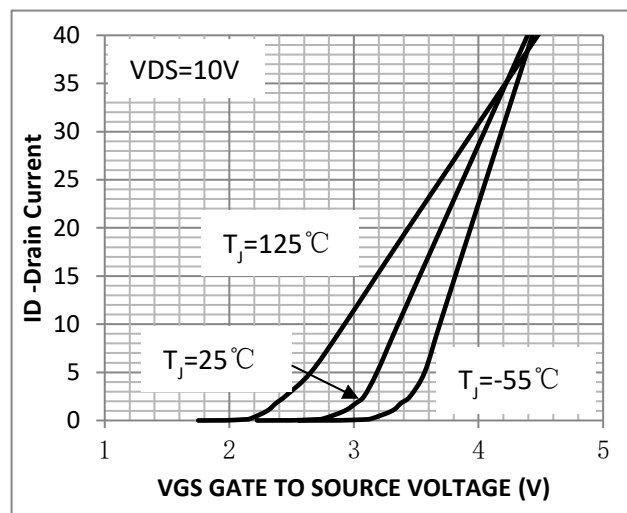


Fig.7 Switching Time Measurement Circuit

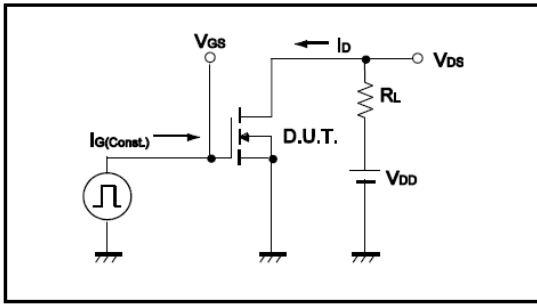


Fig.8 Gate Charge Waveform

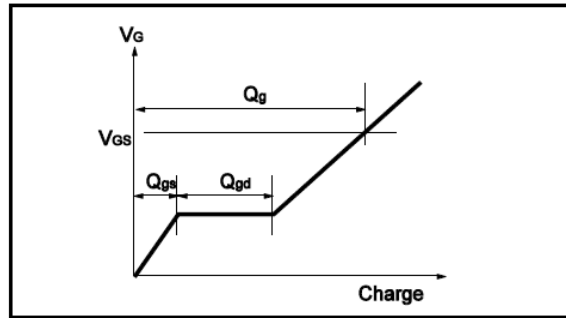


Fig.9 Switching Time Measurement Circuit

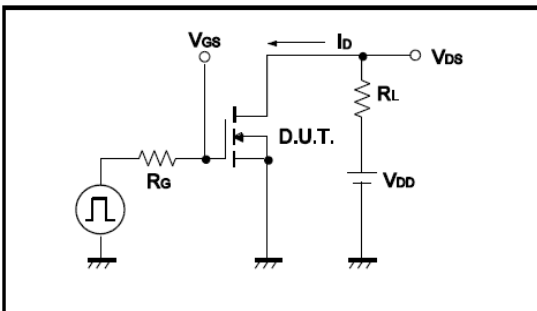


Fig.10 Gate Charge Waveform

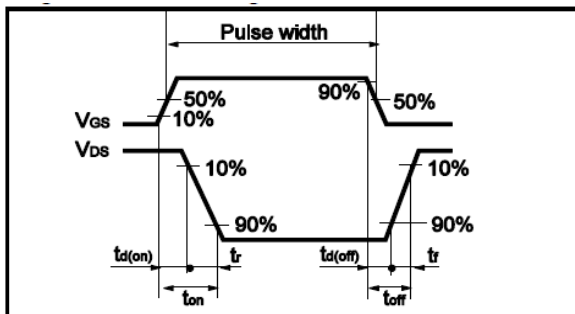


Fig.11 Avalanche Measurement Circuit

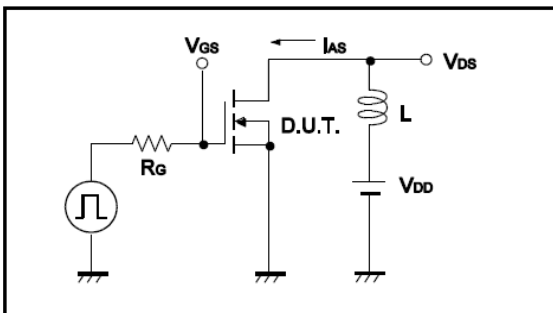
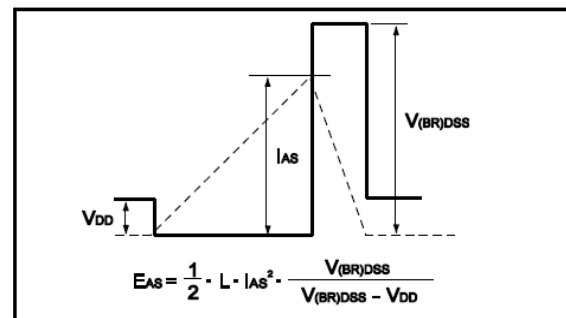
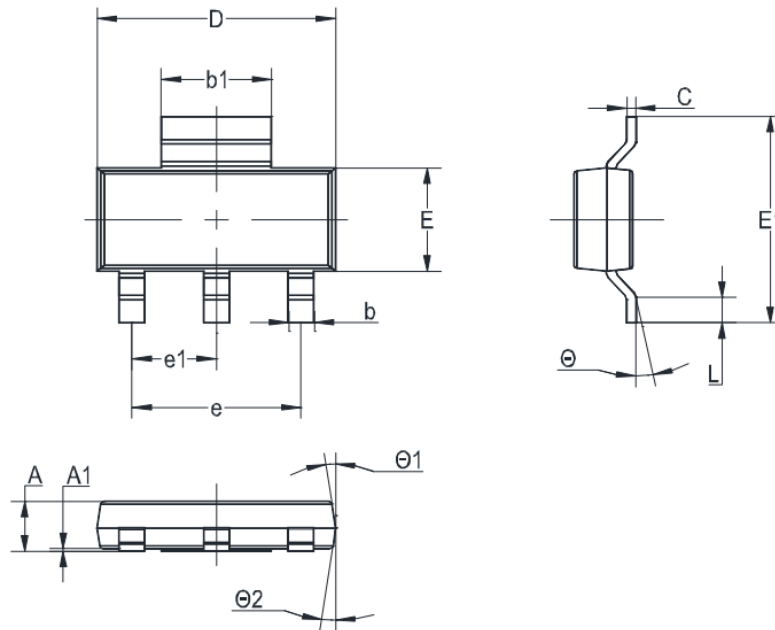


Fig.12 Avalanche Waveform

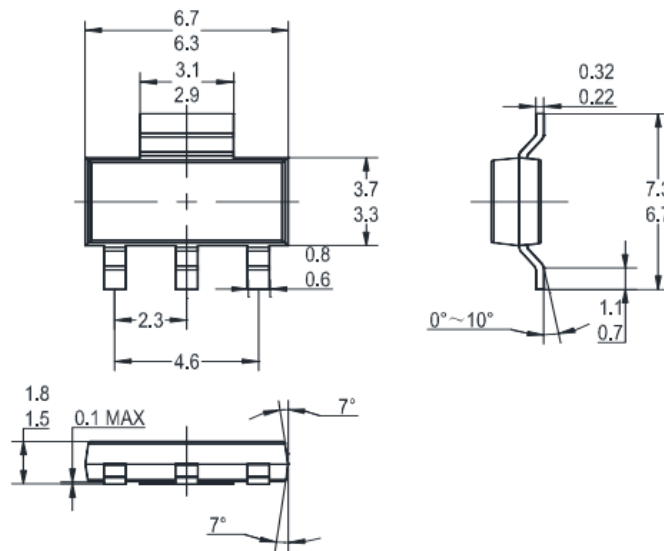


•Dimensions(SOT-223)

Unit: mm

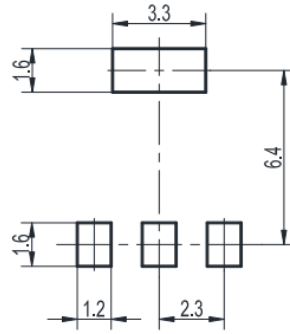


Unit	A	A1	b	b1	C	D	E	E1	e	e1	L	Θ	Θ1	Θ2
mm	1.8	0.1	0.8	3.1	0.32	6.7	3.7	7.3	4.6	2.3	1.1	10°	7°	7°
	1.5	MAX	0.6	2.9	0.22	6.3	3.3	6.7	TYP	TYP	0.7	0°	0°	0°





Recommended Soldering Footprint



Packing information

Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
SOT-223	12	8 ± 0.1	0.315 ± 0.004	330	13	3,000



Note: ① Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$;

② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;

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